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05/06/98 JC408 U.S. PTO

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PTO/SB/05 (1/98)
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Patent and Trademark Office: U S. DEPARTMENT OF COMMERCE

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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	2915.1US (96-149.01)
First Inventor or Application Identifier	Pan, et al.
Title	Technique for Elimination of Pitting on Silicon Substrate During Gate Stack Etch
Express Mail Label No.	EM548957369US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] * Fee Transmittal Form (e.g., PTO/SB/17) (Submit an original, and a duplicate for fee processing)
2. [X] Specification [Total Pages 16] (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings (if filed)
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) (35 U.S.C. 113) [Total Sheets 14]
4. Oath or Declaration [Total Pages 2]
   - a. [ ] Newly executed (original or copy)
   - b. [X] Copy from a prior application (37 C.F.R. § 1.63(d)) (for continuation/divisional with Box 17 completed) [Note Box 5 below]
     - i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).
5. [ ] Incorporation By Reference (useable if Box 4b is checked) The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein
6. [ ] Microfiche Computer Program (Appendix)
7. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
   - a. [ ] Computer Readable Copy
   - b. [ ] Paper Copy (identical to computer copy)
   - c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 C F R §3 73(b) Statement (when there is an assignee) [ ] Power of Attorney
10. [ ] English Translation Document (if applicable)
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copies of IDS Citations
12. [X] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. [ ] * Small Entity Statement(s) (PTO/SB/09-12) [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. [ ] Other ....

* A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.

17. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment.

[ ] Continuation [X] Divisional [ ] Continuation-in-part (CIP) of prior application No: 08 / 682,935

Prior application information: Examiner H. Nguyen Group / Art Unit: 2812

18. CORRESPONDENCE ADDRESS

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Signature	Robert G. Winkle	Date	5/6/98

PTO/SB/17 (1/98)
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FEE TRANSMITTAL

Patent fees are subject to annual revision on October 1. These are the fees effective October 1, 1997. Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid See Forms PTO/SB/09-12

TOTAL AMOUNT OF PAYMENT ($) 872

Complete if Known	
Application Number	
Filing Date	May 6, 1998
First Named Inventor	Pan, et al.
Examiner Name	
Group / Art Unit	
Attorney Docket No	2915.1US (96-149.01)

METHOD OF PAYMENT (check one)

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number: 20-1469

Deposit Account Name: Trask Britt & Rossa

[X] Charge Any Additional Fee Required Under 37 CFR 1 16 and 1 17

[ ] Charge the Issue Fee Set in 37 CFR 1 18 at the Mailing of the Notice of Allowance

2. [X] **Payment Enclosed:** [X] Check [ ] Money Order [ ] Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	790	201	395	Utility filing fee	790
106	330	206	165	Design filing fee	
107	540	207	270	Plant filing fee	
108	790	208	395	Reissue filing fee	
114	150	214	75	Provisional filing fee	
				SUBTOTAL (1)	($) 790

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims	6	-20** =	0	X	0	=	0
Independent Claims	4	- 3** =	1	X	82	=	82
Multiple Dependent						=	

**or number previously paid, if greater; For Reissues, see below*

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	22	203	11	Claims in excess of 20
102	82	202	41	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	82	209	41	** Reissue independent claims over original patent
110	22	210	11	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 82

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	950	217	475	Extension for reply within third month	
118	1,510	218	755	Extension for reply within fourth month	
128	2,060	228	1,030	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,320	241	660	Petition to revive - unintentional	
142	1,320	242	660	Utility issue fee (or reissue)	
143	450	243	225	Design issue fee	
144	670	244	335	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))	
149	790	249	395	For each additional invention to be examined (37 CFR 1.129(b))	

Other fee (specify) ______________________

Other fee (specify) ______________________

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($)

SUBMITTED BY

Typed or Printed Name	Robert G. Winkle	Reg Number	37,474
Signature	[signature] Date 5/6/98	Deposit Account User ID	20-1469

Burden Hour Statement. This form is estimated to take 0 2 hours to complete Time will vary depending upon the needs of the individual case Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231 DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS SEND TO: Assistant Commissioner for Patents, Washington, DC 20231

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Pan et al.

Serial No.: 08/682,935

Filed: July 16, 1996

For: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON SUBSTRATE DURING GATE STACK ETCH

Examiner: H. Nguyen

Group Art Unit: 2812

Attorney Docket No.: 2915US(96-0149)

NOTICE OF EXPRESS MAILING
Express Mail Mailing Label Number 548957369US
Date of Deposit with USPS: May 6, 1998
Person mailing Deposit: Timothy W. Ricks

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination of the claims on the merits in the above-identified application, please amend this application as follows:

IN THE CLAIMS:

Please cancel claims 1-22.

REMARKS

No new subject matter has been introduced with these amendments.

Entry of the above preliminary amendment is respectfully requested. This amendment is submitted prior to the issuance of the first Office action. No new matter has been added.

Respectfully submitted,

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Date: May 6, 1998
RGW/cw
N:\2269\2915\prelim.amd

PATENT
Attorney Docket 2915US(96-0149)

CERTIFICATION UNDER 37 C.F R. § 1 10

EM083912113US	July 16, 1996
Express Mail Mailing Label No.	Date of Deposit

I hereby certify that this application is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on the date indicated above and is addressed to Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Mathew Allen	
Typed or printed name of person mailing application	Signature of person mailing application

APPLICATION FOR LETTERS PATENT

for

TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON SUBSTRATE DURING GATE STACK ETCH

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TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON SUBSTRATE DURING GATE STACK ETCH

BACKGROUND OF THE INVENTION

Field of the Invention: The present invention relates to a method for forming a gate stack which minimizes or eliminates damage to the gate dielectric layer and/or the silicon substrate during gate stack formation. More particularly, the present invention relates to reducing temperature during the fabrication of the gate stack to eliminate the formation of silicon clusters within the metallic silicide film of the gate stack. The present invention also includes methods for dispersing silicon clusters prior to the gate etch step.

State of the Art: The operating speed of semiconductor devices in very large scale integration ("VSLI") and ultra large scale integration ("USLI") depends primarily on the resistivity of the conductive material (hereinafter "trace material") used to transmit signals from one circuit component to another circuit component. Additionally, in order to increase the circuit component density and/or reduce the complexity of the metal connections between the circuit components, a highly conductive trace material layer is required on the gate stack. Thus, the trace material must be a low-resistivity material.

Metallic silicides have recently become popular for use as low-resistivity trace material. Tungsten silicide ("WSi_x") has become a leading low-resistivity trace material. Various etching chemistries have been developed to pattern the WSi_x to form such conductors as the digitlines or wordlines used in memory devices (see, commonly-owned U.S. Patent 5,492,597 hereby incorporated herein by reference). Other metallic silicides used in gate stacks include cobalt silicide ("$CoSi_x$"), molybdenum silicide ("$MoSi_x$"), and titanium silicide ("$TiSi_x$"). These metallic silicides have lower resistivity and are easier to fabricate than other conductors used for this purpose. However, metallic silicides are prone to oxidization. Furthermore, the metal components of the metallic silicides react chemically when they contact other elements. These properties present several problems, including degradation of

the semiconductor element and peeling of the metallic silicide film. To compensate for these problems, a polysilicon layer is usually disposed between a gate dielectric layer and the metallic silicide film, and a dielectric cap layer is usually disposed above the metallic silicide film to isolate the metallic silicide.

FIGS. 14-19 illustrate, in cross section, a conventional method of forming a gate stack having a metallic silicide film layer. FIG. 14 illustrates a gate dielectric layer 204 such as silicon dioxide (SiO_2) grown (by oxidation) or deposited (by any known industry standard technique, such chemical vapor deposition or the like) on a silicon substrate 202. A polysilicon layer 206 is formed on top of the gate dielectric layer 204, as shown in FIG. 15. The polysilicon layer 206 is then subjected to an ion implantation with gate impurities (not shown). As shown in FIG. 16, a metallic silicide film 208 is deposited on the polysilicon layer 206. The structure 118 is then subjected to a heat treatment for about 30 minutes at a temperature between about 850° and 950°C for activation of the impurities in the polysilicon layer 206 and to anneal the metallic silicide film 208. The heat treatment temperature level is dictated by the temperature required to anneal the metallic silicide film 208. The annealing of the metallic silicide film 208 is used to reduce its resistivity.

As shown in FIG. 17, a silicon dioxide cap 210 is then deposited on the metallic silicide film 208 at temperatures over 600°C by chemical vapor deposition ("CVD"), low pressure chemical vapor deposition ("LPCVD"), or the like. A resist 212 is then formed and patterned on the silicon dioxide cap 210, as illustrated in FIG. 18. The layered structure is then etched and the resist 212 is stripped to form a gate stack 214, as illustrated in FIG. 19. However, this etching results in pitting on the gate dielectric layer 204. This pitting is illustrated in FIG. 20 wherein a plurality of pits 216 are distributed on the gate dielectric layer 204 between the gate stacks 214.

This pitting is also illustrated in FIG. 19. A pit in the dielectric layer 204 may be shallow, such as shallow pit 218. However, a deep pit, such as deep pit 220, can extend through the gate dielectric layer 204 and into the silicon substrate 202.

The pitting into the silicon substrate 202 will cause junction leakage, refresh problems, and potential destruction of the component. At present, most gate dielectric layers are about 80 Å thick. However, as semiconductor devices continue to be miniaturized, these gate dielectric layers will become thinner. As the gate dielectric layers become thinner, it is more likely that pitting will penetrate through the gate dielectric layer to contact the silicon substrate and cause the aforementioned problems.

Therefore, it would be advantageous to develop a technique which minimizes or eliminates pitting on the gate dielectric layer caused by gate stack etching, while using state-of-the-art semiconductor device fabrication techniques employing known equipment, process steps, and materials.

SUMMARY OF THE INVENTION

The present invention relates to the reduction of the temperature during the fabrication of the gate stack to eliminate the formation of silicon clusters within a metallic silicide film of the gate stack. The elimination of the formation of the silicon clusters minimizes or eliminates damage to the gate dielectric layer and/or silicon substrate during the gate stack formation. The present invention also includes methods for implanting the gate stack layers to disperse the silicon clusters (if they are present in the metallic silicide film) prior to the gate etch step.

One aspect of the method of the present invention begins by forming a gate dielectric layer on a silicon substrate. A polysilicon or amorphous silicon layer (hereinafter "polysilicon layer") is then formed on top of the gate dielectric layer. The polysilicon layer is subjected to an ion implantation with gate impurities and a non-annealed metallic silicide film is thereafter deposited atop the polysilicon layer. A dielectric cap layer is then deposited over the metallic silicide film at a sufficiently low temperature such that the metallic silicide does not anneal. A resist mask is placed over the cap layer and the structure is etched down to the gate dielectric layer to form a gate stack.

Metallic silicides are generally represented by the formula "MSi_x" wherein: "M" is the metal component (i.e., cobalt "Co", molybdenum "Mo", titanium "Ti", tungsten "W", and the like), "Si" is silicon, and "x" is the number of silicon molecules per metal component molecule ("x" is usually between about 2 and 3). Metallic silicide films tend to peel when a low ratio of silicon to metal component is used for gate stack formation (e.g., when "x" is less than 2). In order to reduce the stress of metallic silicide film which causes peeling, a silicon rich metallic silicide film is used in gate stack formation. In particular with the use of WSi_x, an "x" of about 2.3 is preferred.

In prior art techniques, the metallic silicide is annealed to form a crystalline structured metallic silicide film 502, as illustrated in FIG. 23, between a polysilicon layer 504 (atop a gate dielectric layer 506 which is on a silicon substrate 508) and a silicon dioxide layer 510 (below a dielectric cap 512). However, when a silicon rich metallic silicide is used, the annealing step causes the silicon within the metallic silicide to form clusters 514 inside the crystalline structured metallic silicide film 502. These silicon clusters 514 can also form during the subsequent high temperature steps, even if the annealing step does not take place. In specific process terms, the step of forming a dielectric cap over the metallic silicide can exceed 600°C, particularly when deposition techniques such as LPCVD and sputtering are used. These high temperature steps can cause the formation of silicon clusters 514 within the metallic silicide film 502. This can be seen in FIG. 21 wherein a large plurality of pits 304 are formed in the surface of the gate dielectric layer 306 between a plurality of gate stacks 302 (high temperature cap formation only, no annealing step).

It has been found that the pitting on the gate dielectric layer during the full gate stack (cap/metallic silicide/polysilicon) etch is caused by the presence of the silicon clusters inside the metallic silicide film. The etch rate of these silicon clusters has been found to be about 1.2 times that of the metallic silicide film (in the case of tungsten silicide film) during the gate stack etch. Thus, the etch tunnels into the

metallic silicide at each silicon cluster. This tunneling is, in turn, translated into the surface of the gate dielectric layer, thereby forming the pits.

By preventing the growth and formation of the silicon clusters in the metallic silicide film, the problem of pitting on the silicon substrate during the gate stack etch can be eliminated. Although prior art techniques anneal the metallic silicide film to reduce its resistivity and consequentially forming the undesirable silicon clusters, it has been found that, for most purposes, the metallic silicide film has sufficiently low resistivity without annealing. Thus, one aspect of the method of the present invention eliminates annealing the metallic silicide film. Although the step of annealing the metallic silicide film also activates gate impurities, the activation of the gate impurities can be completed during subsequent heat cycles after the etching of the gate stack, such as during shallow junction formation.

In a preferred variation of the method, the dielectric cap is selectively deposited on an upper surface of the metallic silicide film at low temperatures. The dielectric cap material is preferably silicon nitride. The deposition of the silicon nitride layer is carried out at between about 400 and 600°C, which temperature does not anneal the metallic silicide film, and thus does not result in the growth and formation silicon clusters in the metallic silicide film. It is of course understood that the cap can include silicon dioxide layers, or the like, so long as deposition is performed at temperatures below about 600°C. Forming the cap by selectively depositing silicon nitride by plasma-enhanced chemical vapor deposition ("PECVD") is also preferred, since only one surface of the substrate is covered by the dielectric material which eliminates the necessity of removing the cap material from the semiconductor substrate back surface, thus providing a process cost advantage.

FIG. 24 is a side cross-sectional view of a layered gate stack structure of the present invention prior to etching, depicting of a silicon nitride cap 602, a silicon dioxide layer 604, a metallic silicide film 606, a polysilicon layer 608, a gate dielectric layer 610, and a silicon substrate 612. Since no high temperature cycle occurs during the layered gate stack structure formation, the metallic silicide film 606

does not form a crystalline structure, nor does it contain silicon clusters. Thus, as illustrated in FIG. 22, the method of the present invention does not initiate damage or pitting on the gate dielectric layer 402 during the etching and formation of the gate stacks 404.

In situations where a high temperature heat cycle (cap deposition and/or annealing) is required, an ion implantation into the metallic silicide film can be performed to amorphize the metallic silicide film (i.e., disperse the silicon clusters back into the metallic silicide film) before masking and etching. The implantation ions can be silicon, tungsten, argon, or the like, or a dopant (phosphorous, arsenic, boron, and the like). The implantation can be performed before and/or after the cap deposition. The implantation energy is preferably between about 20 keV and 200 keV. The ion dose ranges from between about $1E^{13}$ and $1E^{16}$. The implantation energy and dose depend on the metallic silicide film thickness, the metallic silicide composition (i.e., ratio of silicon to metal component), the anneal heat cycle temperature, and the implantation ion used. However, it is preferred that the peak of the implantation occur at about the middle of the metallic silicide film. Furthermore, it is preferred that the dopant ion (phosphorous, arsenic, boron, and the like) amorphize the metallic silicide film. For example, for a metallic silicide film which is about 1800Å thick and annealed at about 850°C for about 30 minutes, a phosphorous implantation at about 75 keV and $1E^{15}$ is required to amorphize the metallic silicide.

It is, of course, understood that if a lower resistivity in the metallic silicide is required for a specific application, the gate stack can be subjected to a heat cycle after gate stack etching to anneal the metallic silicide in the gate stack. However, if the gate stack is annealed after formation, the anneal temperature must be increased by about 30 to 50°C to achieve the same resistivity.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming that which is regarded as the present invention, the advantages of this invention can be more readily ascertained from the following description of the invention when read in conjunction with the accompanying drawings in which:

FIGS. 1-6 are side cross-sectional views of a gate stack formation method of the present invention;

FIGS. 7-13 are side cross-sectional views of an alternate gate stack formation method of the present invention;

FIGS. 14-19 are side cross-sectional views of a prior art gate stack formation method;

FIG. 20 is an oblique view of a gate stack and a pitted gate dielectric layer formed by a prior art method with annealing and high temperature cap formation;

FIG. 21 is an oblique view of a gate stack and a pitted gate dielectric layer formed by a prior art method with high temperature cap formation;

FIG. 22 is an oblique view of a gate stack and a gate dielectric layer formed by the present invention;

FIG. 23 is a side cross-sectional view of a prior art gate stack structure prior to etching; and

FIG. 24 is a side cross-sectional view of a gate stack structure of the present invention prior to etching.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIGS. 1-6 illustrate a method, in cross section, of forming a gate stack of the present invention. FIG. 1 illustrates a gate dielectric layer 104 such as silicon dioxide formed on a silicon substrate 102. A polysilicon layer 106 is formed on top of the gate dielectric layer 104, as shown in FIG. 2. The polysilicon layer 106 is then subjected to an ion implantation with gate impurities (not shown). As shown in FIG. 3, a metallic silicide film 108 is deposited on the polysilicon layer 106. The

metallic silicide film can be deposited by CVD (including LPCVD, APCVD, and PECVD), sputtering, or the like.

A cap 110, preferably including silicon nitride, is then deposited on the metallic silicide film 108, as shown in FIG. 4. The deposition of the silicon nitride layer is carried out at between about 400 and 600°C, and preferably at about 500°C, by CVD (including LPCVD, APCVD, and PECVD), sputtering, spin-on techniques, or the like. In a preferred embodiment, the deposition of the silicon nitride is accomplished by plasma-enhanced chemical vapor deposition. It is, of course, understood that the cap 110 can include other dielectric material such as silicon dioxide, as long as it deposited at temperatures below about 600°C.

A resist 112 is then formed and patterned on the cap 110, as illustrated in FIG. 5. The structure is then etched and the resist 112 stripped to form a gate stack 114, as shown in FIG. 6.

FIGS. 7-13 illustrate an alternate method, in cross section, of forming a gate stack of the present invention. The steps of the alternate method are similar to the method illustrated in FIGS. 1-6, therefore components common to both FIGS. 1-6 and FIG. 7-13 retain the same numeric designation. FIG. 7 illustrates a gate dielectric layer 104 grown or deposited on a silicon substrate 102. A polysilicon layer 106 is formed on top of the gate dielectric layer 104, as shown in FIG. 8. The polysilicon layer 106 is then subjected to an ion implantation with gate impurities (not shown). As shown in FIG. 9, a metallic silicide film 108 is deposited on the polysilicon layer 106. A cap 110 is then deposited on the metallic silicide film 108, as shown in FIG. 10. The structure 118 is subjected to a heat cycle either to anneal the metallic silicide film 108 prior to depositing the cap 110, to form the cap 110 with a high temperature process (i.e., over 600°C), or both, such that silicon clusters 116 are formed in the metallic silicide film 108.

As shown in FIG. 11, the structure 118 is subjected to an implantation 120 which disperses the silicon clusters 116 back into the metallic silicide film 108. The implantation 120 can be ions of silicon, tungsten, argon, or the like, or a dopant

(phosphorous, arsenic, boron, and the like). The implantation 120 can be performed before and/or after the cap deposition. A resist 112 is then formed and patterned on the cap 110, as illustrated in FIG. 12. The structure 118 is then etched and the resist 112 stripped to form a gate stack 114, as shown in FIG. 13.

* * * * *

Having thus described in detail preferred embodiments of the present invention, it is to be understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description as many apparent variations thereof are possible without departing from the spirit or scope thereof.

CLAIMS

What is claimed is:

1. A method for forming a metallic silicide film and dielectric cap during a gate stack formation wherein said gate stack includes a polysilicon layer, comprising:

forming said metallic silicide film in a non-annealed state over said polysilicon layer; and

forming said dielectric cap on said metallic silicide film at sufficiently low temperature that said metallic silicide film remains in said non-annealed state.

2. The method of claim 1 wherein forming said dielectric cap occurs at a temperature below about 600°C.

3. A method for forming a gate stack, comprising:

providing a semiconductor substrate with a dielectric layer on an active surface of said semiconductor substrate, wherein a polysilicon layer is disposed over said dielectric layer;

forming a metallic silicide film in a non-annealed state over said polysilicon layer;

forming a dielectric cap on said metallic silicide film at a sufficiently low temperature that said metallic silicide film remains in said non-annealed state;

forming and patterning a resist layer on said dielectric cap;

etching said dielectric cap, said metallic silicide film, and said polysilicon layer; and stripping said resist layer.

4. The method of claim 3 wherein forming said dielectric cap occurs at a temperature below about 600°C.

5. In a method of forming a gate stack wherein a layered structure is fabricated by forming a dielectric layer on an active surface of a semiconductor

substrate, forming a polysilicon layer on said dielectric layer, forming a metallic silicide film on said polysilicon layer, forming a dielectric cap on said metallic silicide film, forming and patterning a resist layer on said dielectric cap, etching said layered structure, an stripping said resist layer, the improvement comprising:

forming a metallic silicide film in a non-annealed state over said polysilicon layer; and

forming a dielectric cap on said metallic silicide film at sufficiently low temperature that said metallic silicide film remains in said non-annealed state.

6. The method of claim 5 wherein forming said dielectric cap occurs at a temperature below about 600°C.

7. A method for forming a gate stack, comprising the steps of:

forming a layered structure, comprising the steps of:

providing a semiconductor substrate having a dielectric layer on an active surface thereof with a polysilicon layer disposed over said dielectric layer,

forming a metallic silicide film over said polysilicon layer, and

forming a dielectric cap on said metallic silicide film;

subjecting at least said metallic silicide film of said layered structure to at least one heat cycle during said forming of said layered structure;

implanting said layered structure;

forming and patterning a resist layer on said dielectric cap;

etching said dielectric cap, said metallic silicide film, and said polysilicon layer; and

stripping said resist layer.

8. The method of claim 7, wherein implanting said layered structure comprises ion implantation.

9. The method of claim 8, wherein said ion implantation comprises implantation of ions selected from the group consisting of silicon, tungsten, and argon.

10. The method of claim 7, wherein implanting said layer structure comprises doping.

11. The method of claim 10, wherein said doping comprises doping with a dopant selected from the group consisting of phosphorous, arsenic, and boron.

12. The method of claim 7, wherein said at least one heat cycle occurs after said formation of said metallic silicide film on said polysilicon layer to anneal said metallic silicide film.

13. The method of claim 7, wherein said at least one heat cycle occurs during said formation of said dielectric cap on said metallic silicide film.

14. The method of claim 7, wherein said at least one heat cycle includes a temperature of at least 600°C.

15. In a method of forming a gate stack wherein a layered structure is fabricated by forming a dielectric layer on an active surface of a semiconductor substrate, forming a polysilicon layer on said dielectric layer, forming a metallic silicide film on said polysilicon layer, forming a dielectric cap on said metallic silicide film, subjecting at least said metallic silicide film of said layered structure to at least one heat cycle resulting in the formation of undesired silicon clusters within said metallic silicide film, forming and patterning a resist layer on said dielectric cap, etching said layered structure, and stripping said resist layer, the improvement

comprising implanting said layered structure to disperse said undesired silicon clusters prior to etching said layered structure.

16. The method of claim 15, wherein implanting said layer structure comprises ion implantation.

17. The method of claim 16, wherein said ion implantation comprises implantation of ions selected from the group consisting of silicon, tungsten, and argon.

18. The method of claim 15, wherein implanting said layer structure comprises doping.

19. The method of claim 18, wherein said doping comprises doping with a dopant selected from the group consisting of phosphorous, arsenic, and boron.

20. The method of claim 15, wherein said at least one heat cycle occurs after said formation of said metallic silicide film on said polysilicon layer to anneal said metallic silicide film.

21. The method of claim 15, wherein said at least one heat cycle occurs during said formation of said dielectric cap on said metallic silicide film.

22. The method of claim 15, wherein said at least one heat cycle includes a temperature of at least 600°C.

23. A gate stack, including a metallic silicide film in a non-annealed state.

24. A gate stack, including a metallic silicide film in an annealed state wherein said metallic silicide is substantially devoid of silicon clusters.

25. A gate stack on a dielectric layered semiconductor substrate, comprising:

a polysilicon layer disposed over said dielectric layered semiconductor substrate;

a metallic silicide film in a non-annealed state disposed over said polysilicon layer; and

a dielectric cap on said metallic silicide film formed at a sufficiently low temperature that said metallic silicide film remains in said non-annealed state.

26. A gate stack structure comprising a gate stack on a dielectric layered semiconductor substrate wherein said dielectric layer is substantially devoid of pitting.

27. The gate stack structure of claim 26 wherein said a gate stack includes a non-annealed metallic silicide film.

28. The gate stack structure of claim 26 wherein said a gate stack includes an annealed metallic silicide film.

ABSTRACT

A method for forming a gate stack which minimizes or eliminates damage to the gate dielectric layer and/or silicon substrate during the gate stack formation by the reduction of the temperature during formation. The temperature reduction prevents the formation of silicon clusters within the metallic silicide film in the gate stack which has been found to cause damage during the gate etch step. The present invention also includes methods for dispersing silicon clusters prior to the gate etch step.

FIG. 1

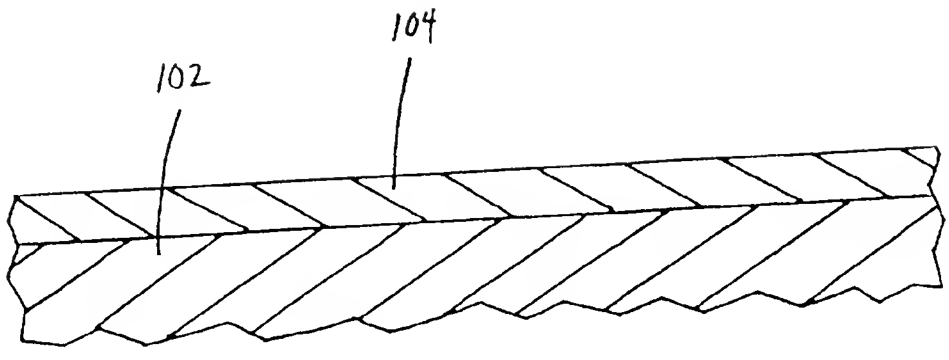

FIG. 2

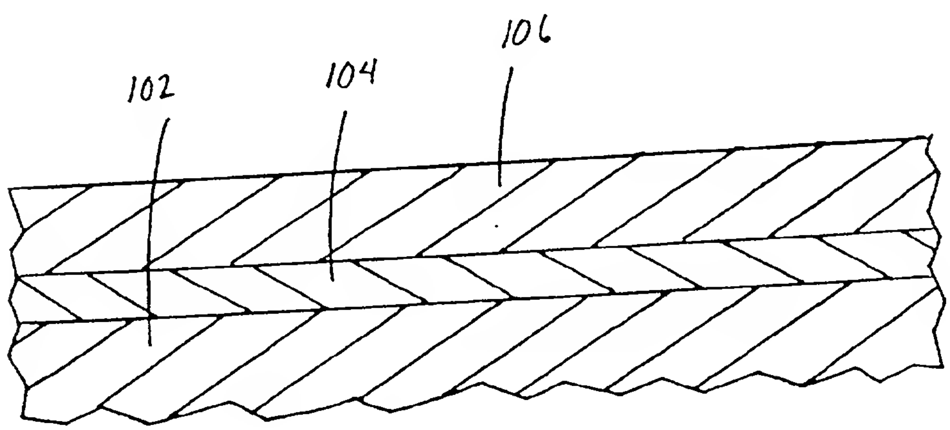

FIG. 3

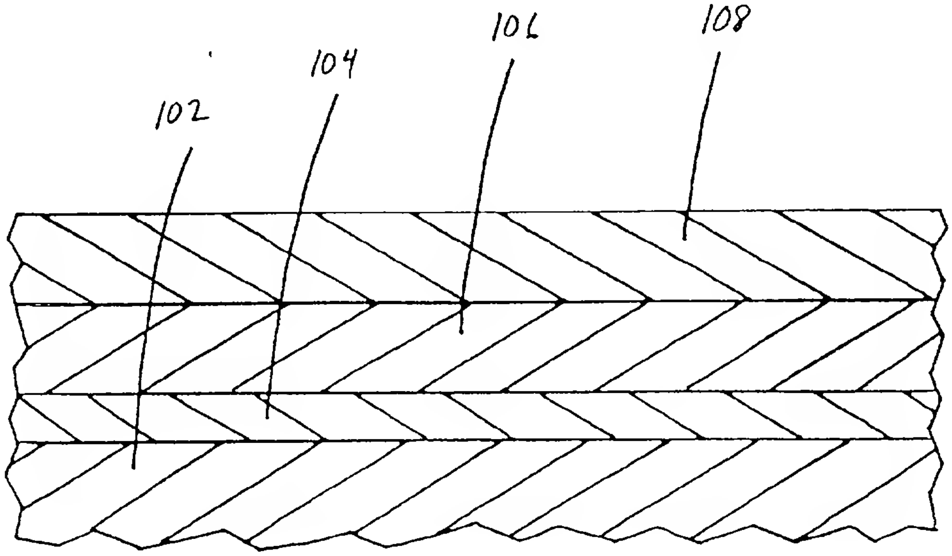

FIG. 4

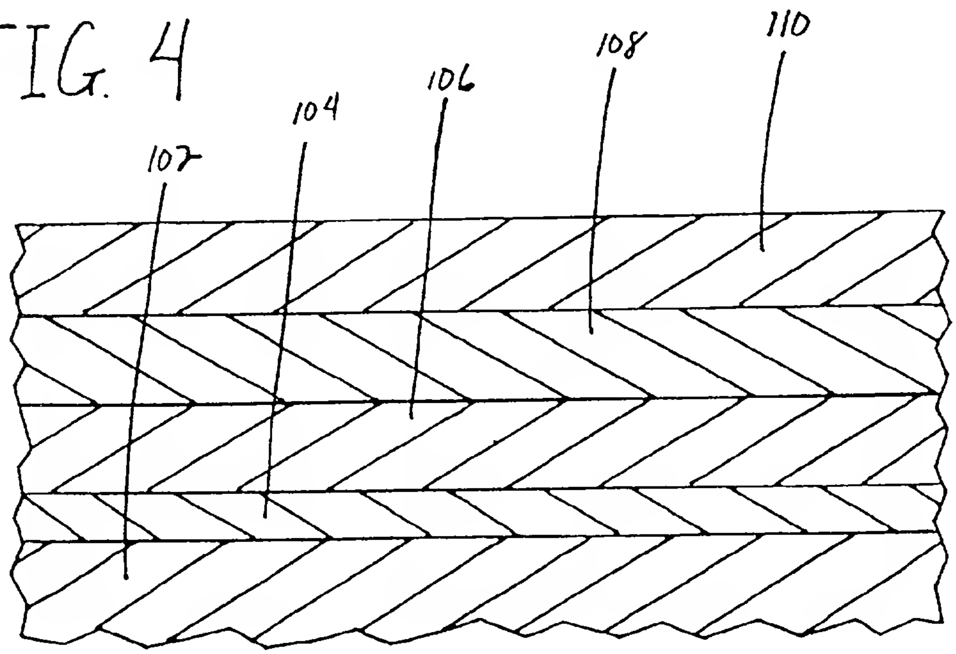

FIG. 5

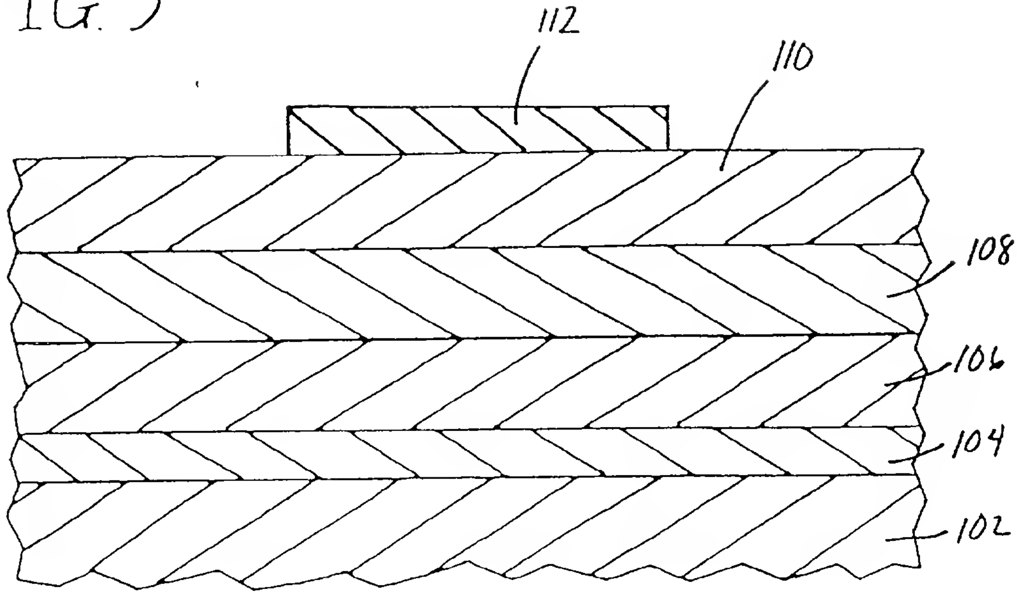

FIG. 6

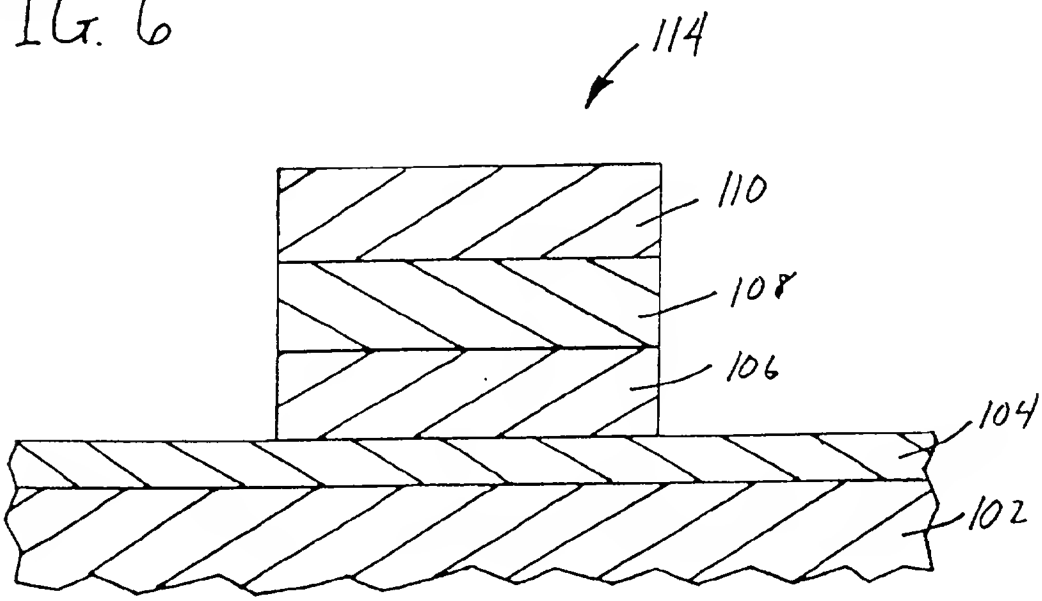

FIG. 1

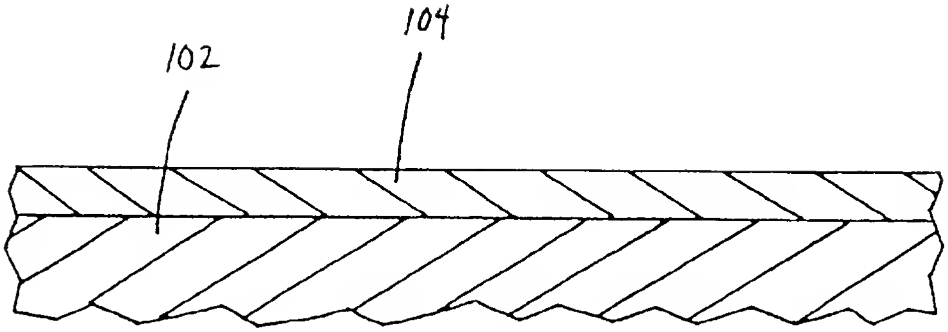

FIG. 2

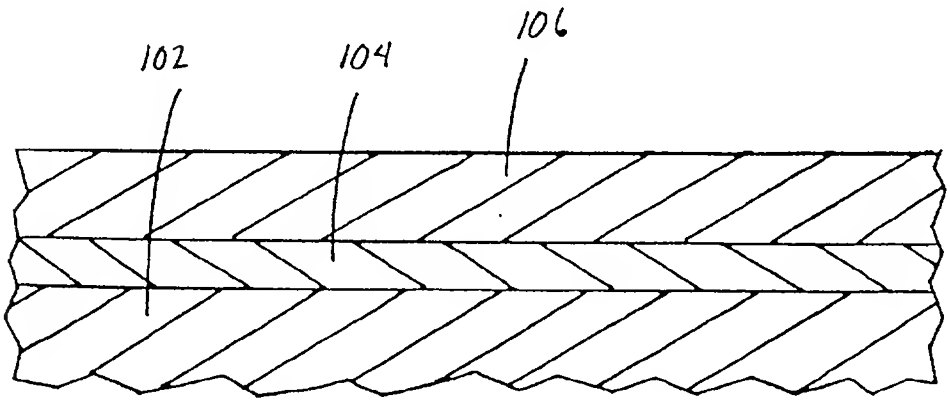

FIG. 7

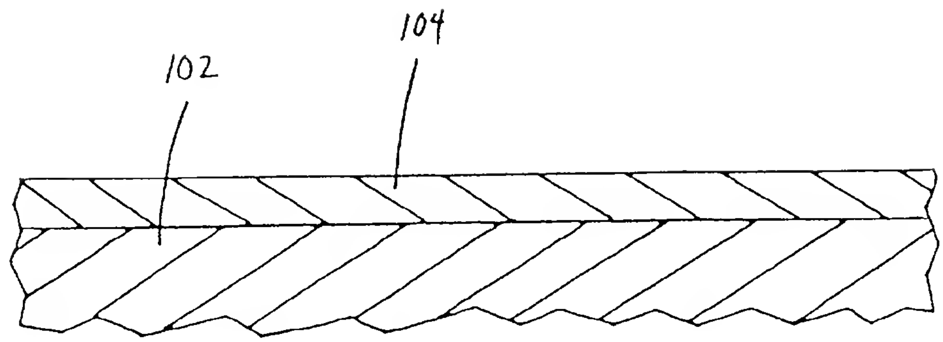

FIG. 8

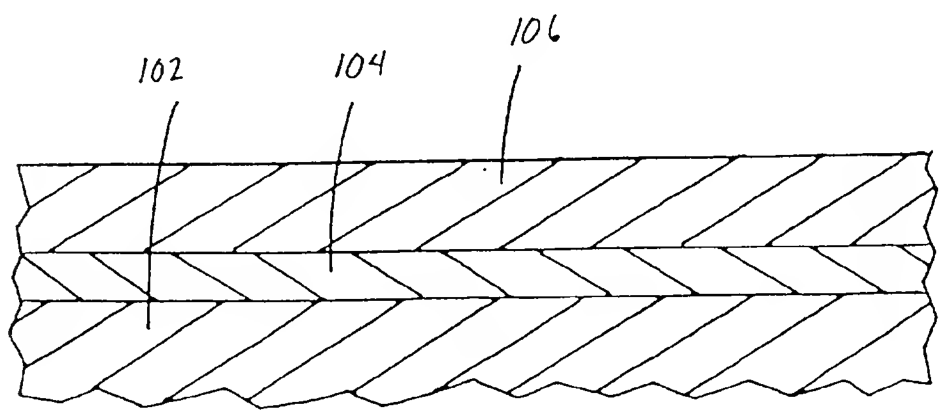

FIG. 9

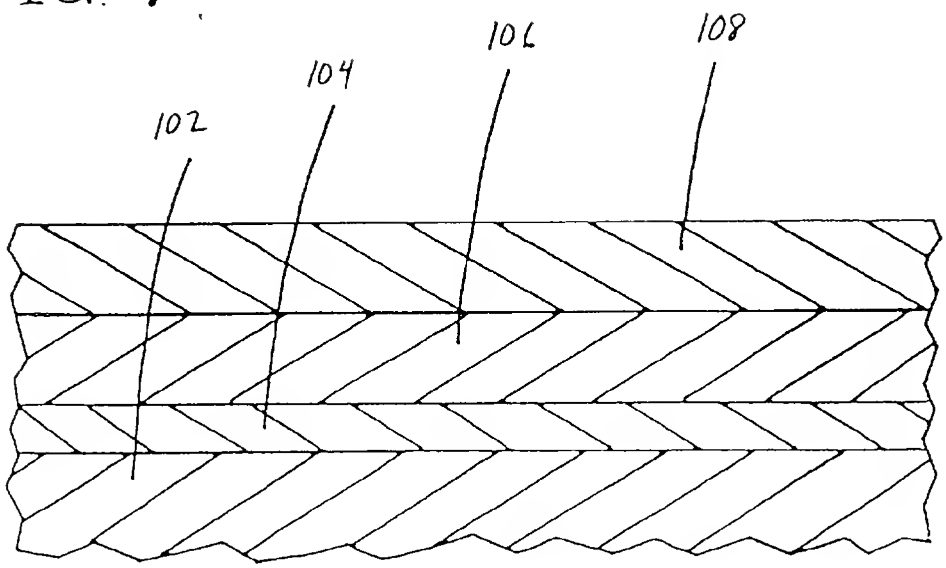

FIG. 10

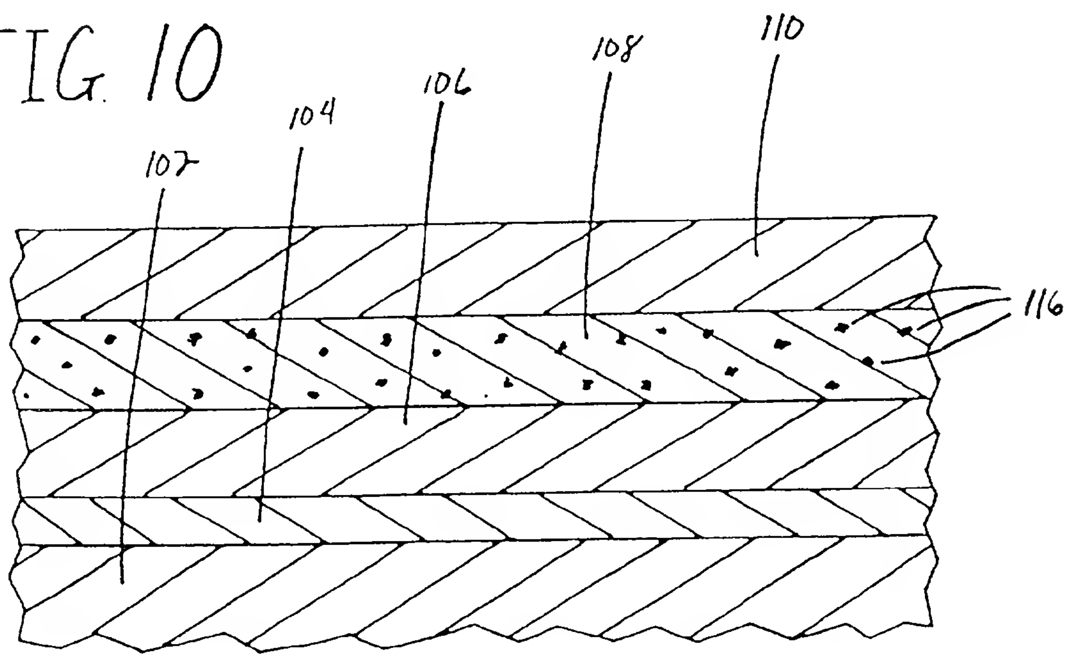

FIG. 11

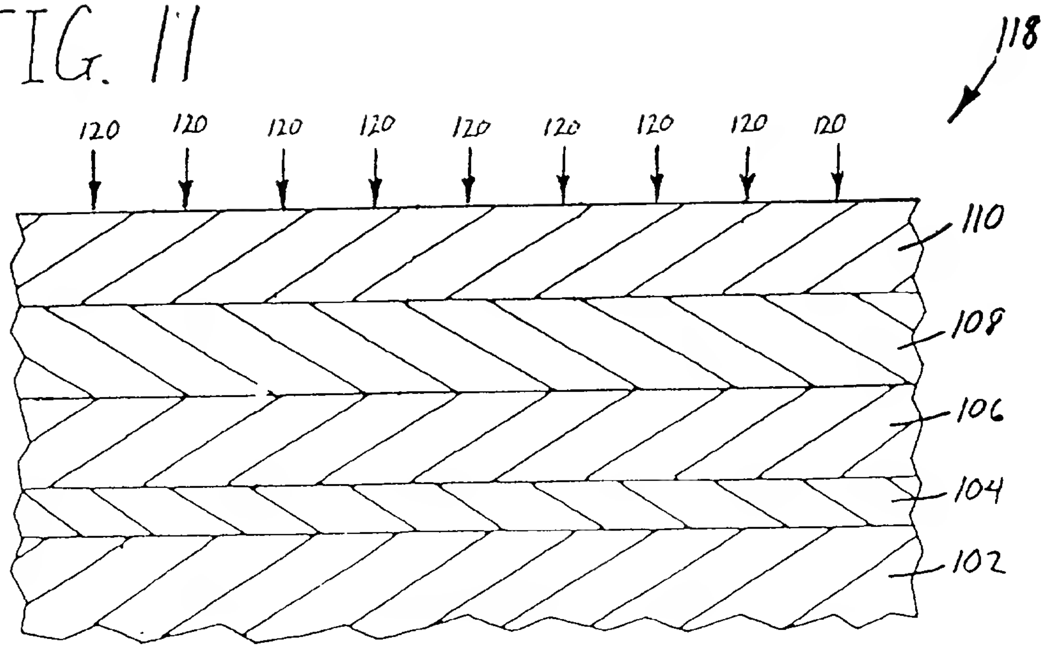
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FIG. 12

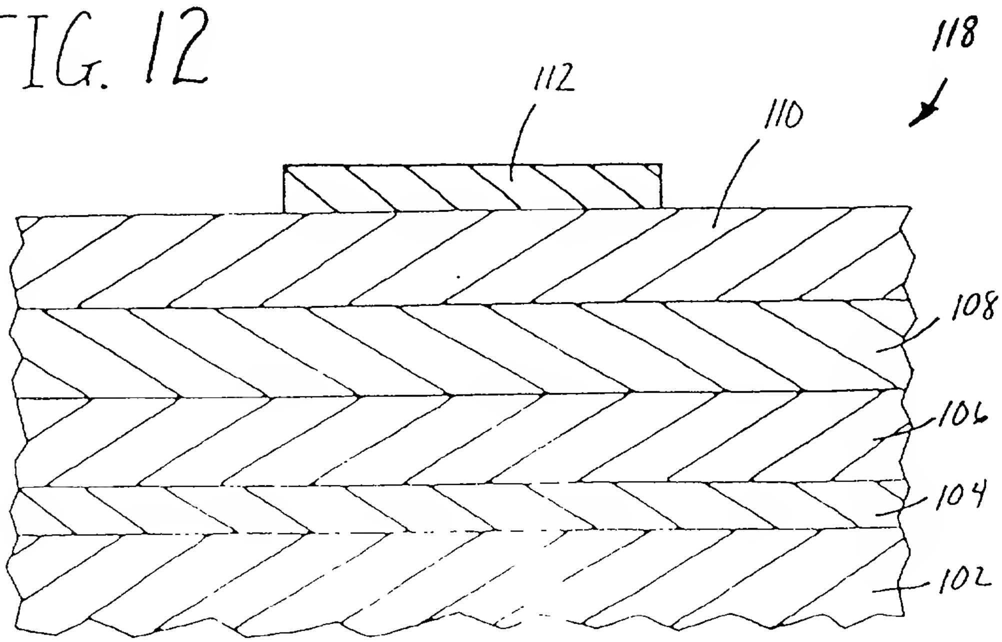
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FIG. 13

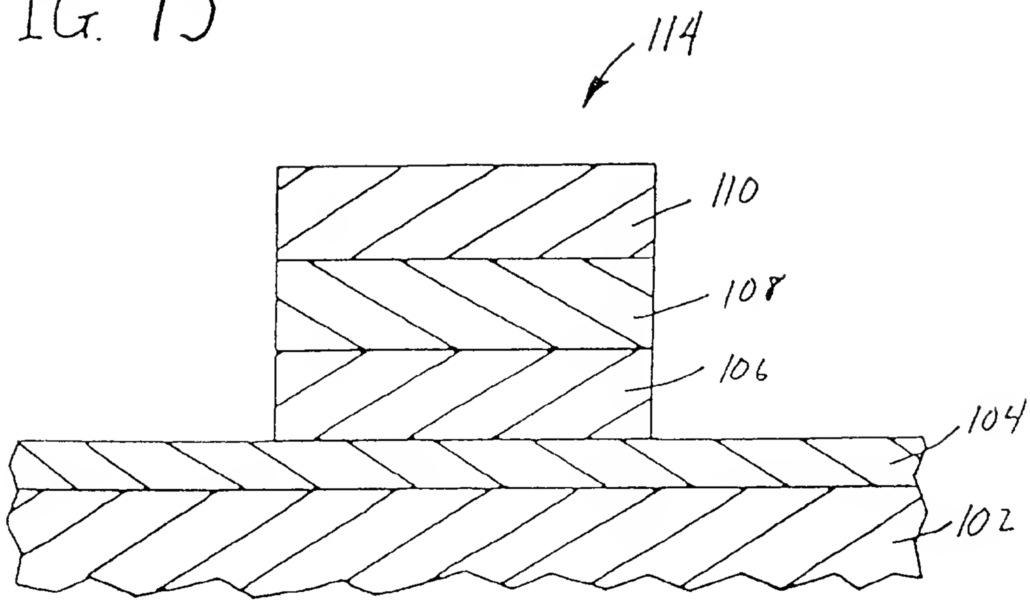


FIG. 14
PRIOR ART

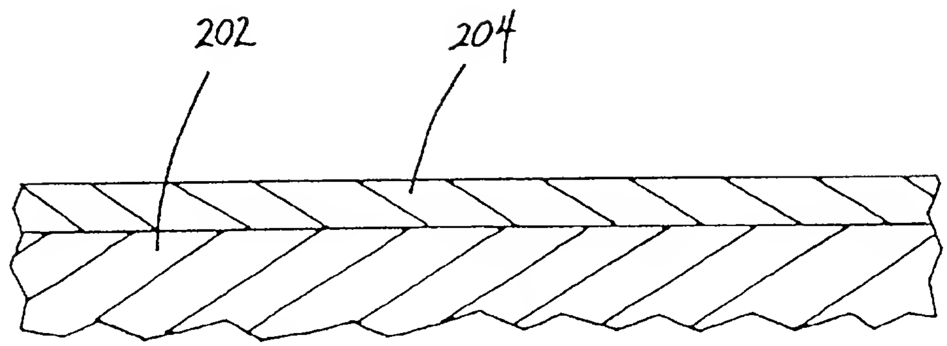


FIG. 15
PRIOR ART

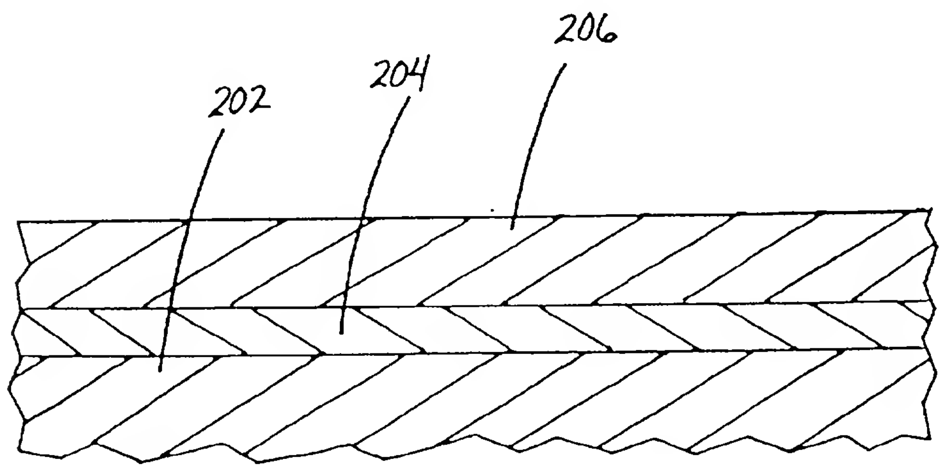


FIG. 16

PRIOR ART

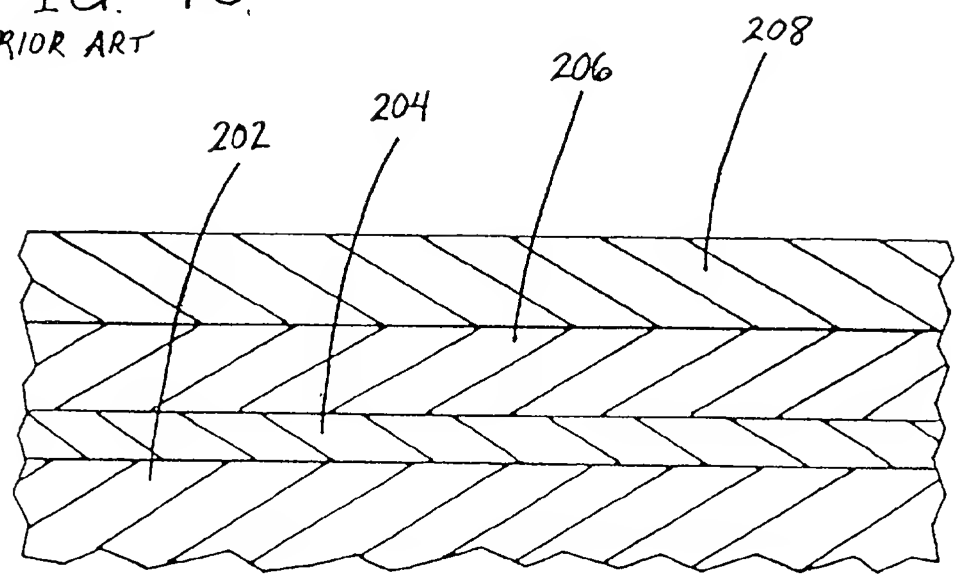


FIG. 17

PRIOR ART

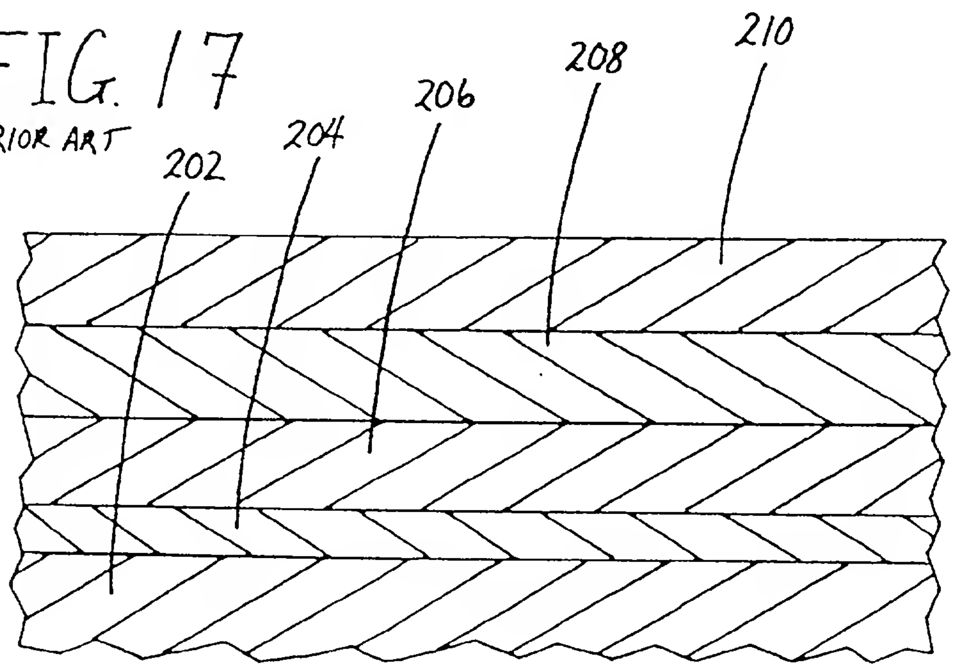


FIG. 18
PRIOR ART

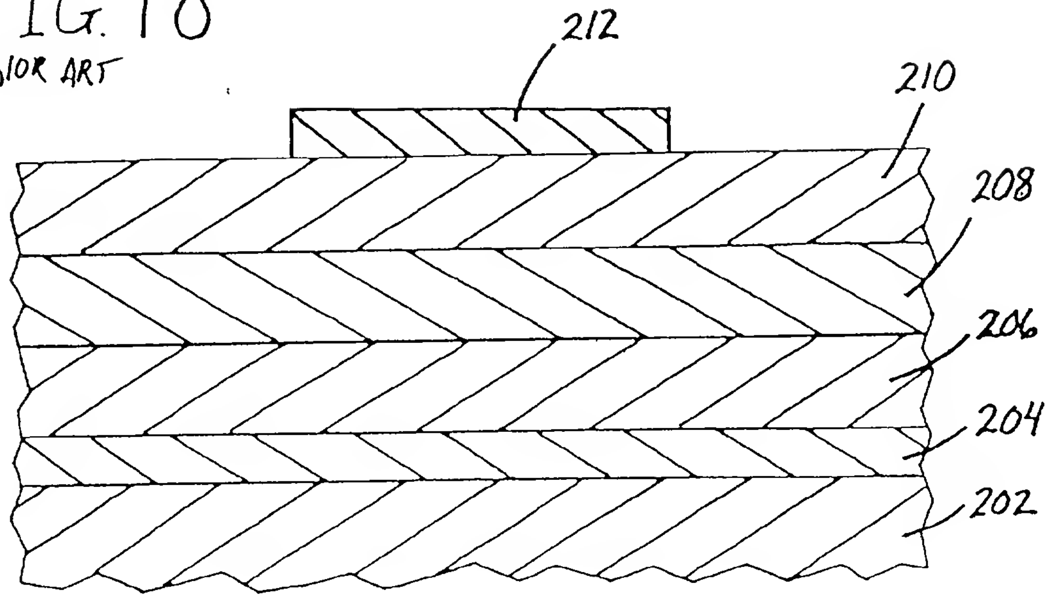


FIG. 19
PRIOR ART

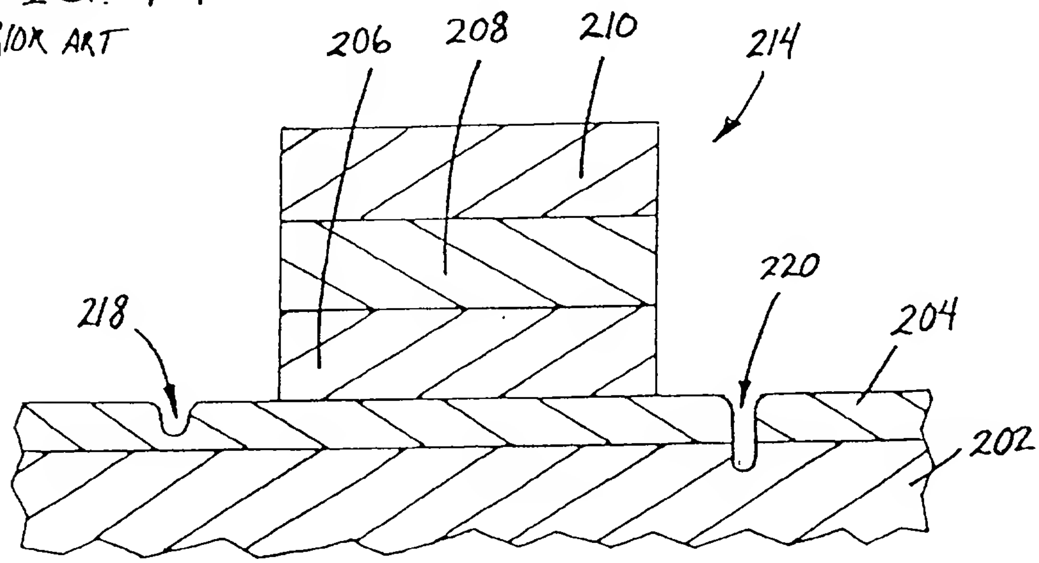


FIG. 20

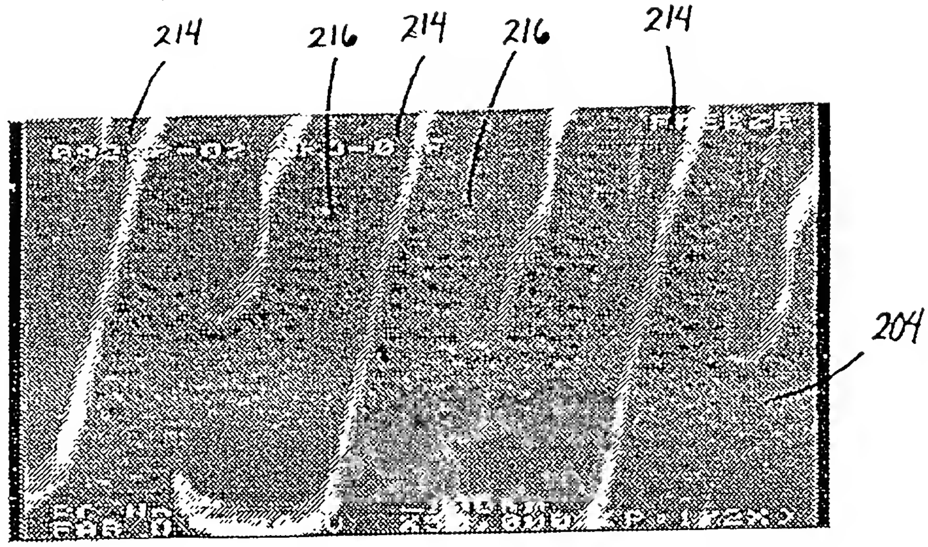


FIG. 21

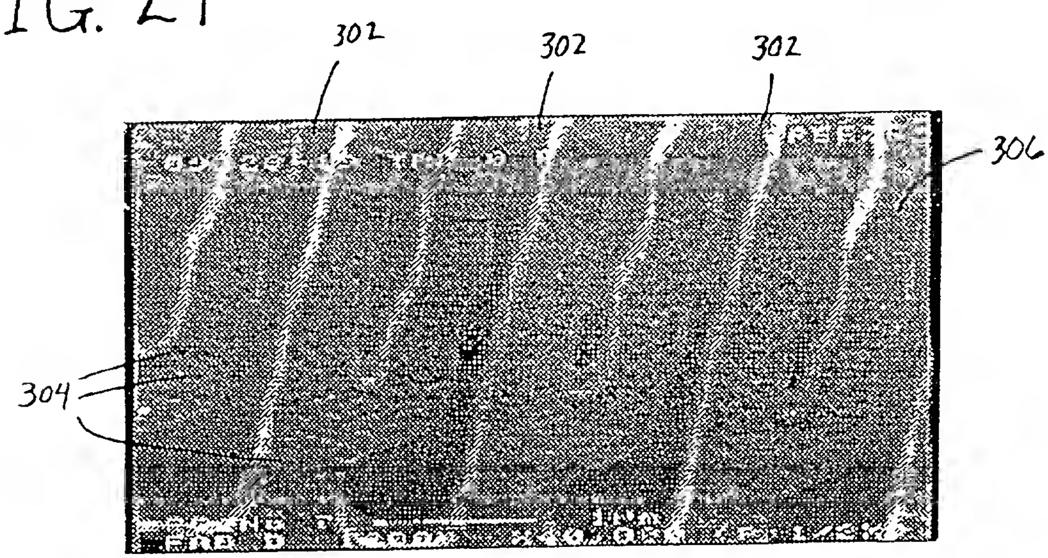
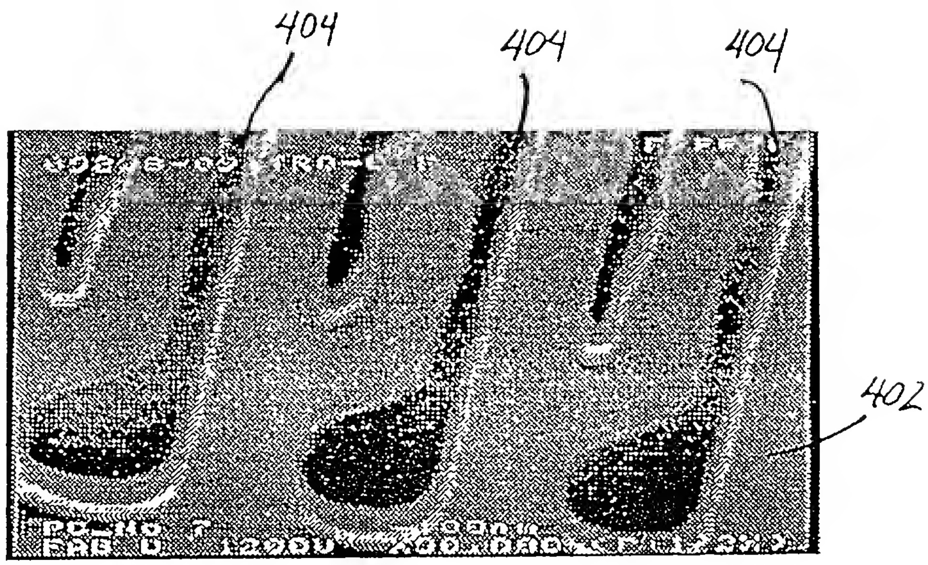


FIG. 22



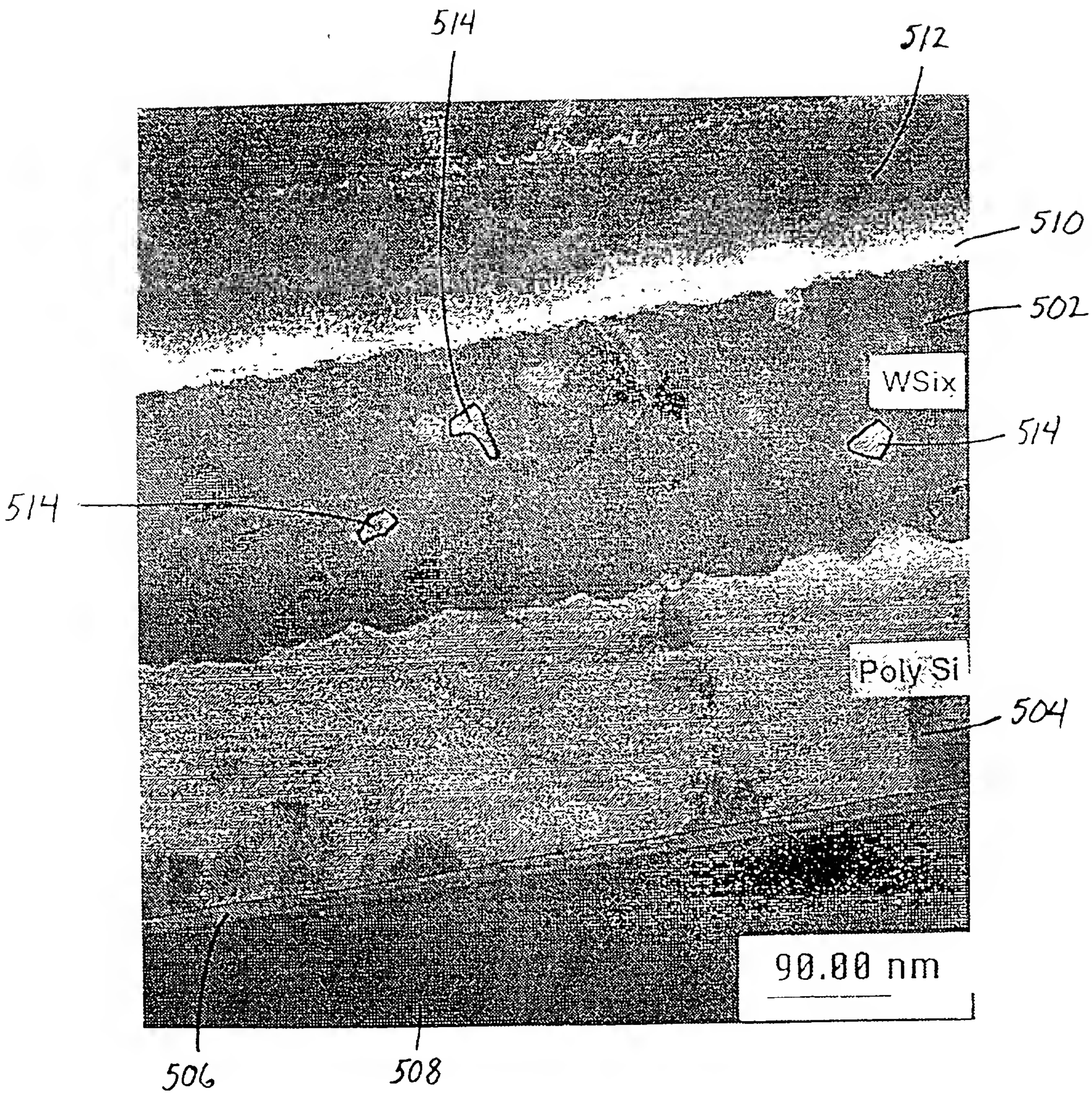


FIG. 23

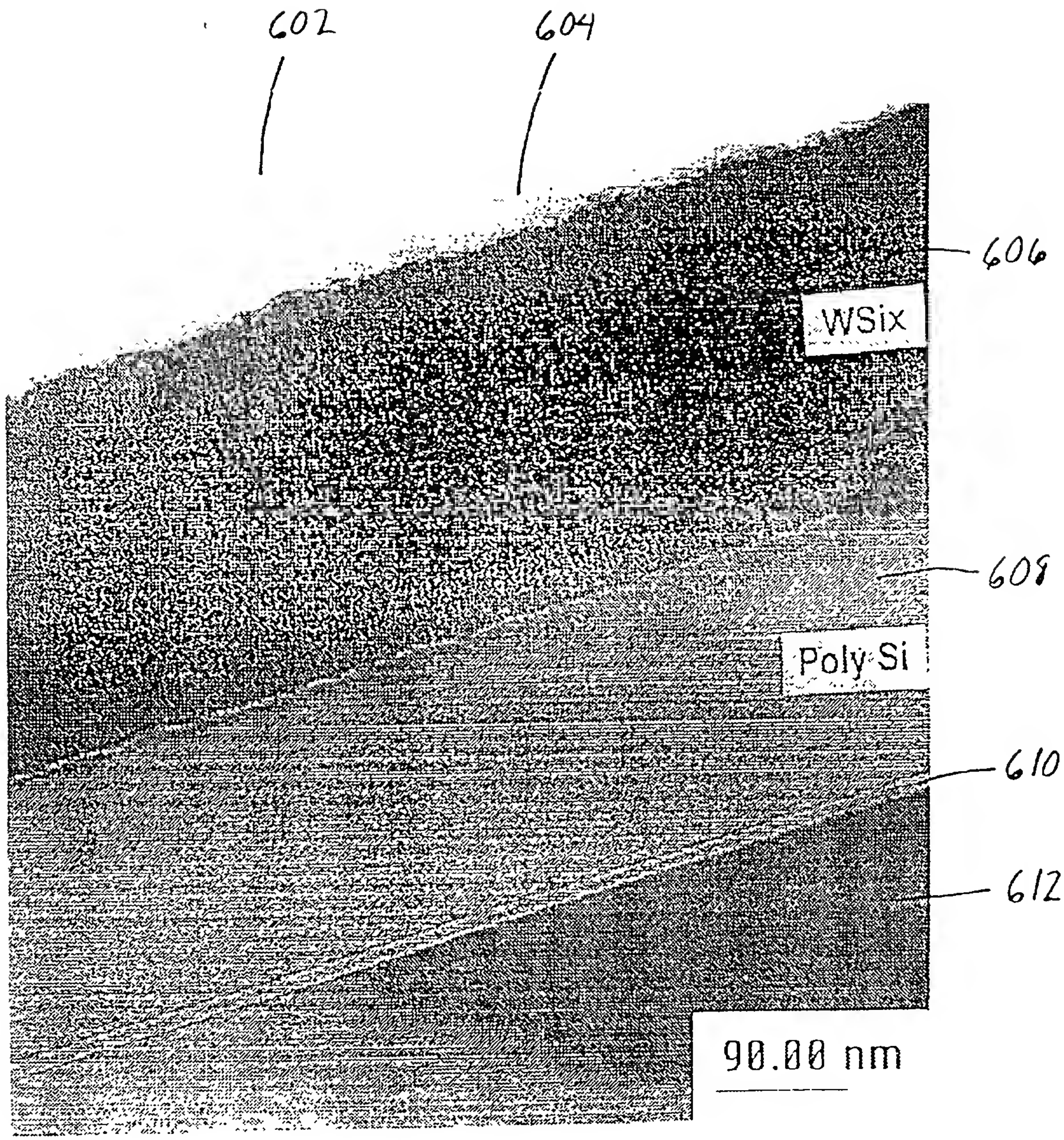


FIG. 24

DECLAR. N FOR PATENT APPLICATION (WITH POWER OF ˉORNEY)

As an inventor named below or on any attached continuation page, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON SUBSTRATE DURING GATE STACK ETCH, the specification of which (check one):

- ☐ is attached hereto.
- ☒ was filed on 07/16/96 as United States application serial no. 08/682,935 and was amended on .
- ☐ was filed on __________ as PCT international application no. __________ and was amended under PCT Article 19 on __________.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 (a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT international application(s) designating at least one country other than the United States of America listed below and on any attached continuation page and have also identified below and on any attached continuation page any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America having a filing date before that of the application(s) on which priority is claimed.

Prior foreign/PCT application(s):

			Priority Claimed	
(number)	(country)	(day/month/year filed)	Yes	No
(number)	(country)	(day/month/year filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or § 365(c) of PCT international application(s) designating the United States of America listed below and on any attached continuation page and, insofar as the subject matter of each of the claims of this application is not disclosed in any such prior application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of such prior application and the national or PCT international filing date of this application:

(application serial no.)	(filing date)	(status - pending, patented or abandoned)
(application serial no.)	(filing date)	(status - pending, patented or abandoned)

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

(provisional application no.)	(filing date)
(provisional application no.)	(filing date)
(provisional application no.)	(filing date)

I hereby appoint the following Registered Practitioners to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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TRASK, BRITT & ROSSA
P.O. BOX 2550
Salt Lake City, Utah 84110

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's signature Pai-Hung Pan Date 10-07-96
Residence: Boise, Idaho
Citizenship: U.S.A.
Post Office Address: 2773 East Migratory Drive, Boise, Idaho 83706

DECLARATION FOR PATENT APPLICATION
(continuation page)

Invention title: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON SUBSTRATE DURING GATE STACK ETCH

Inventor name(s) appearing on first declaration page: Pai-Hung Pan

☒ Additional original, first and joint inventor(s):

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Inventor's signature Louie Liu Date 10-01-96
Residence: Meridian, Idaho
Citizenship: Taiwan
Post Office Address: 1412 N. Sandlin Avenue, Meridian, Idaho 83642

Full name of third joint inventor: Ravi Iyer
Inventor's signature Ravi Iyer Date 10/02/96
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Citizenship: India
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